

## WHAT IS CLAIMED IS:

1. A semiconductor integrated device comprising:

a single or plurality of logic circuits each including  
5 a first circuit for inputting a clock signal and a second circuit  
operating in synchronization with said clock signal input by  
said first circuit;

a first power supply wire connected with said first  
circuit of each said logic circuit; and

10 a second power supply wire provided independently of said  
first power supply wire and connected with said second circuit  
of each said logic circuit.

2. The semiconductor integrated circuit according to  
15 claim 1, further comprising:

a first input terminal for externally supplying a power  
supply voltage to said first power supply wire, and

a second input terminal for externally supplying said  
power supply voltage to said second power supply wire, wherein

20 said first and second input terminals are provided in  
common.

3. The semiconductor integrated circuit according to  
claim 2, further comprising a semiconductor substrate formed  
25 with said single or plurality of logic circuits, said first

power supply wire and said second power supply wire, wherein  
said first and second input terminals include a pad  
electrode formed on said semiconductor substrate in common.

5        4. The semiconductor integrated circuit according to  
claim 1, further comprising:

a first input terminal for externally supplying a power  
supply voltage to said first power supply wire, and

10        a second input terminal for externally supplying said  
power supply voltage to said second power supply wire, wherein  
said first and second input terminals are provided  
independently of each other.

15        5. The semiconductor integrated circuit according to  
claim 4, further comprising a semiconductor substrate formed  
with said single or plurality of logic circuits, said first  
power supply wire and said second power supply wire, wherein  
said first and second input terminals include pad  
electrodes formed on said semiconductor substrate  
20        respectively.

6. The semiconductor integrated circuit according to  
claim 1, wherein

25        said first power supply wire has a larger width than said  
second power supply wire.

7. The semiconductor integrated circuit according to claim 1, wherein

said power supply voltage includes a high-potential side power supply voltage and a low-potential side power supply voltage,

said first power supply wire includes a first high-potential side power supply wire for supplying said high-potential side power supply voltage to said first circuit, and

said second power supply wire includes a second high-potential side power supply wire for supplying said high-potential side power supply voltage to said second circuit,

said semiconductor integrated circuit further comprising a common low-potential side power supply wire for supplying said low-potential side power supply voltage to said first circuit and said second circuit.

8. The semiconductor integrated circuit according to claim 7, further comprising:

a first high-potential side input terminal for externally supplying said high-potential side power supply voltage to said first high-potential side power supply wire,

a second high-potential side input terminal for externally supplying said high-potential side power supply

voltage to said second high-potential side power supply wire,  
and

a low-potential side input terminal for externally  
supplying said low-potential side power supply voltage to said  
5 common low-potential side power supply wire.

9. The semiconductor integrated circuit according to  
claim 8, wherein

said first high-potential side input terminal and said  
10 second high-potential side input terminal are provided in  
common.

10. The semiconductor integrated circuit according to  
claim 8, wherein

15 said first high-potential side input terminal and said  
second high-potential side input terminal are provided  
independently of each other.

11. The semiconductor integrated circuit according to  
20 claim 7, wherein

said first high-potential side power supply wire has a  
larger width than said second high-potential side power supply  
wire.

25 12. The semiconductor integrated circuit according to

claim 7, further comprising:

a semiconductor substrate, and

a multilayer structure, provided on said semiconductor substrate, forming said single or plurality of logic circuits,

5 said first power supply wire and said second power supply wire, wherein

said multilayer structure includes first and second layers,

10 said low-potential side power supply wire is formed on said first layer of said multilayer structure, and

said first and second high-potential side power supply wires are formed on said second layer of said multilayer structure.

15 13. The semiconductor integrated circuit according to claim 1, wherein

said power supply voltage includes a high-potential side power supply voltage and a low-potential side power supply voltage,

20 said first power supply wire includes a first high-potential side power supply wire for supplying said high-potential side power supply voltage to said first circuit and a first low-potential side power supply wire for supplying said low-potential side power supply voltage to said first circuit,

25 and

said second power supply wire includes a second high-potential side power supply wire for supplying said high-potential side power supply voltage to said second circuit and a second low-potential side power supply wire for supplying  
5 said low-potential side power supply voltage to said second circuit.

14. The semiconductor integrated circuit according to claim 13, including:

10 a first high-potential side input terminal for externally supplying said high-potential side power supply voltage to said first high-potential side power supply wire,

a second high-potential side input terminal for externally supplying said high-potential side power supply  
15 voltage to said second high-potential side power supply wire,

a first low-potential side input terminal for externally supplying said low-potential side power supply voltage to said first low-potential side power supply wire, and

a second low-potential side input terminal for  
20 externally supplying said low-potential side power supply voltage to said second low-potential side power supply wire.

15. The semiconductor integrated circuit according to claim 14, wherein

25 said first high-potential side input terminal and said

second high-potential side input terminal are provided in common.

16. The semiconductor integrated circuit according to  
5 claim 14, wherein

said first high-potential side input terminal and said second high-potential side input terminal are provided independently of each other.

10 17. The semiconductor integrated circuit according to claim 14, wherein

said first low-potential side input terminal and said second low-potential side input terminal are provided in common.

15 18. The semiconductor integrated circuit according to claim 14, wherein

said first low-potential side input terminal and said second low-potential side input terminal are provided  
20 independently of each other.

19. The semiconductor integrated circuit according to claim 13, wherein

said first high-potential side power supply wire has a  
25 larger width than said second high-potential side power supply

wire.

20. The semiconductor integrated circuit according to claim 13, wherein

5       said first low-potential side power supply wire has a larger width than said second low-potential side power supply wire.

21. The semiconductor integrated circuit according to claim 13, further comprising:

a semiconductor substrate, and

a multilayer structure, provided on said semiconductor substrate, forming said single or plurality of logic circuits, said first power supply wire and said second power supply wire,  
15       wherein

      said first and second high-potential side power supply wires and said first and second low-potential side power supply wires are formed on the same layer of said multilayer structure.

20       22. The semiconductor integrated circuit according to claim 1, wherein

      said second circuit includes a holding circuit holding the state of an input signal in response to said clock signal input by said first circuit.



23. The semiconductor integrated circuit according to claim 1, wherein

said logic circuit is formed by a basic cell of a standard cell system or a gate array system.